

FIG. 1 is a schematic diagram of a semiconductor device, showing a cross-sectional view of a substrate 10. The substrate 10 is a P-type semiconductor material. A gate stack 12 is formed on the surface of the substrate 10. The gate stack 12 includes a gate dielectric layer 14 and a gate electrode layer 16. The gate electrode layer 16 is connected to a gate terminal 18. The gate stack 12 is divided into two regions, a first region 20 and a second region 22. The first region 20 is a P+ region, and the second region 22 is an N+ region. The first region 20 is connected to a first terminal 24, and the second region 22 is connected to a second terminal 26. The first terminal 24 is connected to a first power supply 28, and the second terminal 26 is connected to a second power supply 30. The first power supply 28 is connected to ground, and the second power supply 30 is connected to a positive voltage source. The substrate 10 is also connected to ground. The gate stack 12 is formed on the surface of the substrate 10, and the gate electrode layer 16 is connected to the gate terminal 18. The gate stack 12 is divided into two regions, a first region 20 and a second region 22. The first region 20 is a P+ region, and the second region 22 is an N+ region. The first region 20 is connected to a first terminal 24, and the second region 22 is connected to a second terminal 26. The first terminal 24 is connected to a first power supply 28, and the second terminal 26 is connected to a second power supply 30. The first power supply 28 is connected to ground, and the second power supply 30 is connected to a positive voltage source. The substrate 10 is also connected to ground.

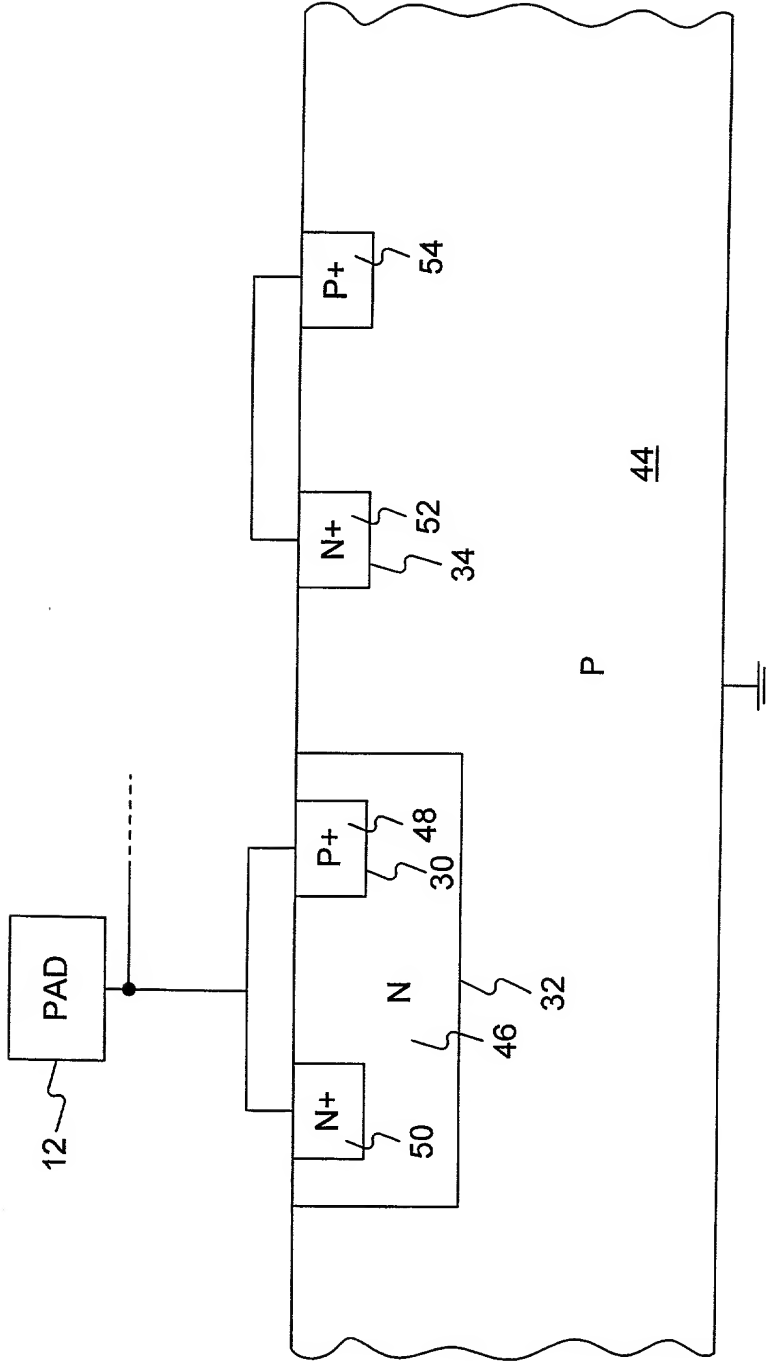


FIG. 1
(Prior Art)

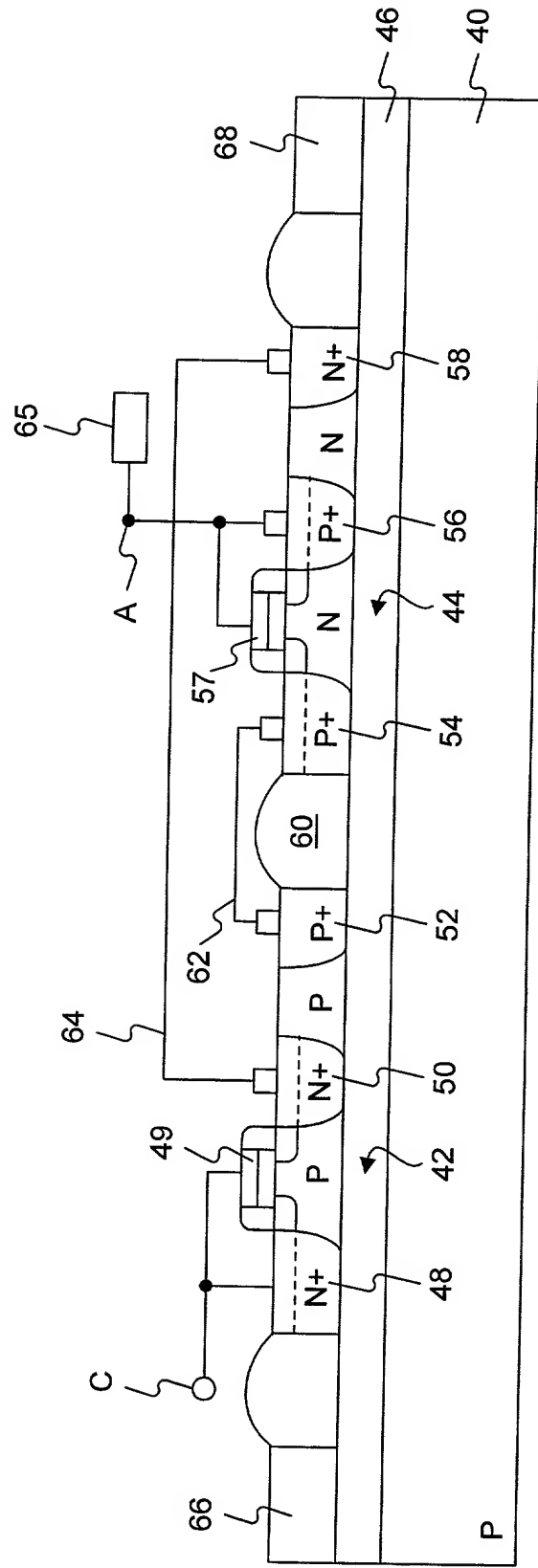


FIG. 2
(Prior Art)

FIG. 6 is a perspective view of a semiconductor device 200 in accordance with one embodiment of the present invention. The device 200 includes a substrate 202, a first gate stack 210, a second gate stack 216, a first source/drain region 208, a second source/drain region 218, a first interlayer dielectric layer 212, a second interlayer dielectric layer 214, a first contact plug 210, a second contact plug 216, a first contact pad 204, a second contact pad 206, and a third contact pad 204.

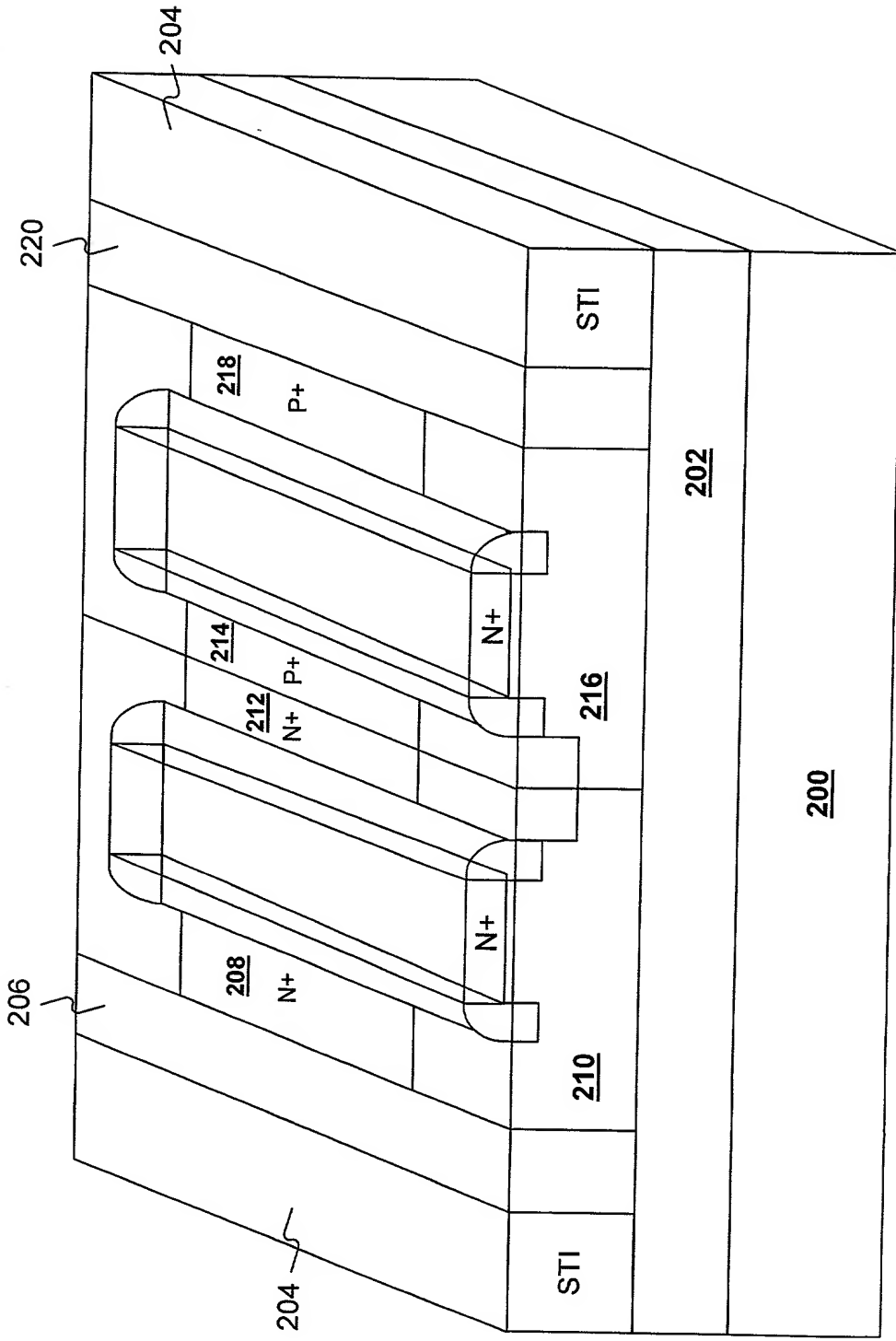


FIG. 6

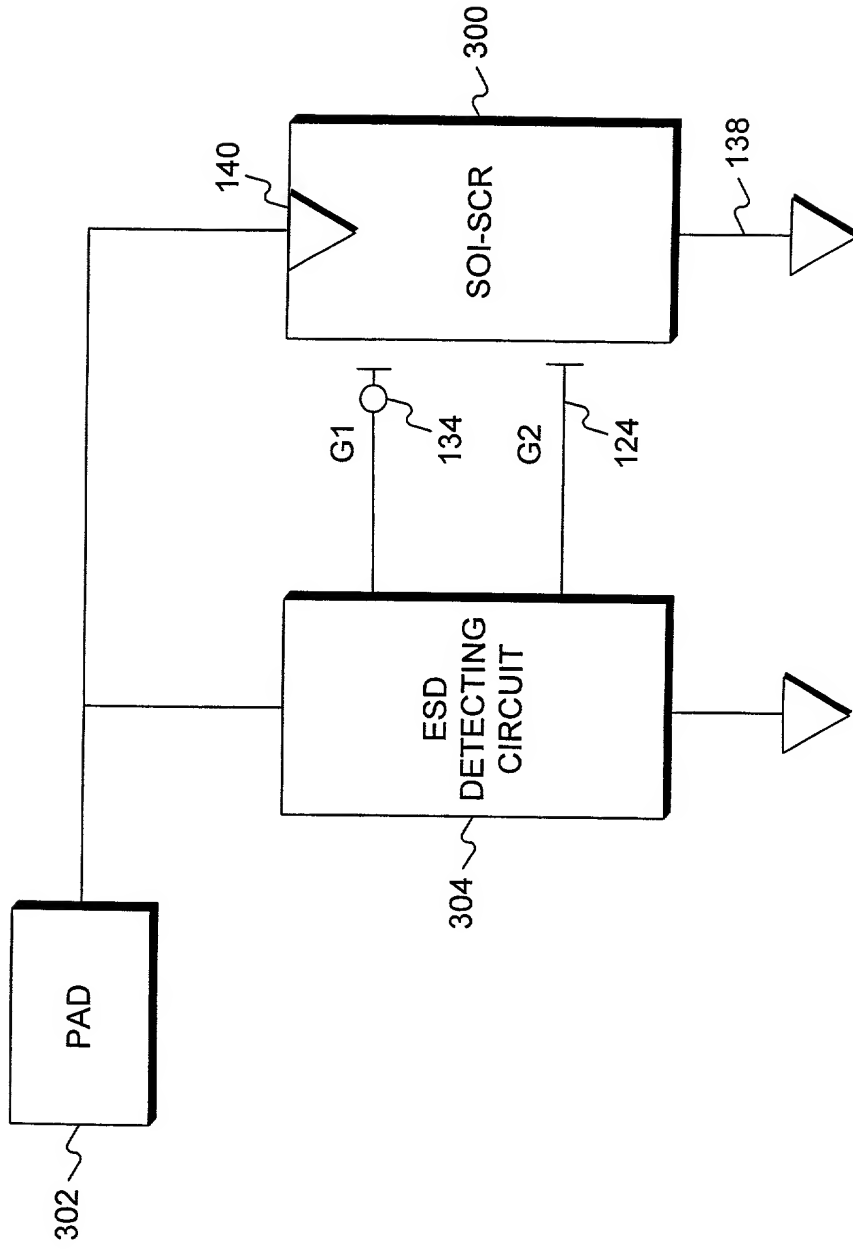


FIG. 7A

FIG. 8A is a schematic diagram of a circuit 300. The circuit 300 includes a first block 304' and a second block 300. The first block 304' is connected to a VDD supply and a VSS supply. The second block 300 is connected to the VDD supply and the VSS supply. A gate G1 is connected to the VDD supply and the first block 304'. A gate G2 is connected to the VDD supply and the second block 300. A node 134 is connected to the VDD supply and the first block 304'. A node 124 is connected to the VDD supply and the second block 300. A node 140 is connected to the VDD supply and the second block 300. A node 138 is connected to the second block 300 and a series of diodes D1, D2, and DN. The diodes D1, D2, and DN are connected to the VSS supply.

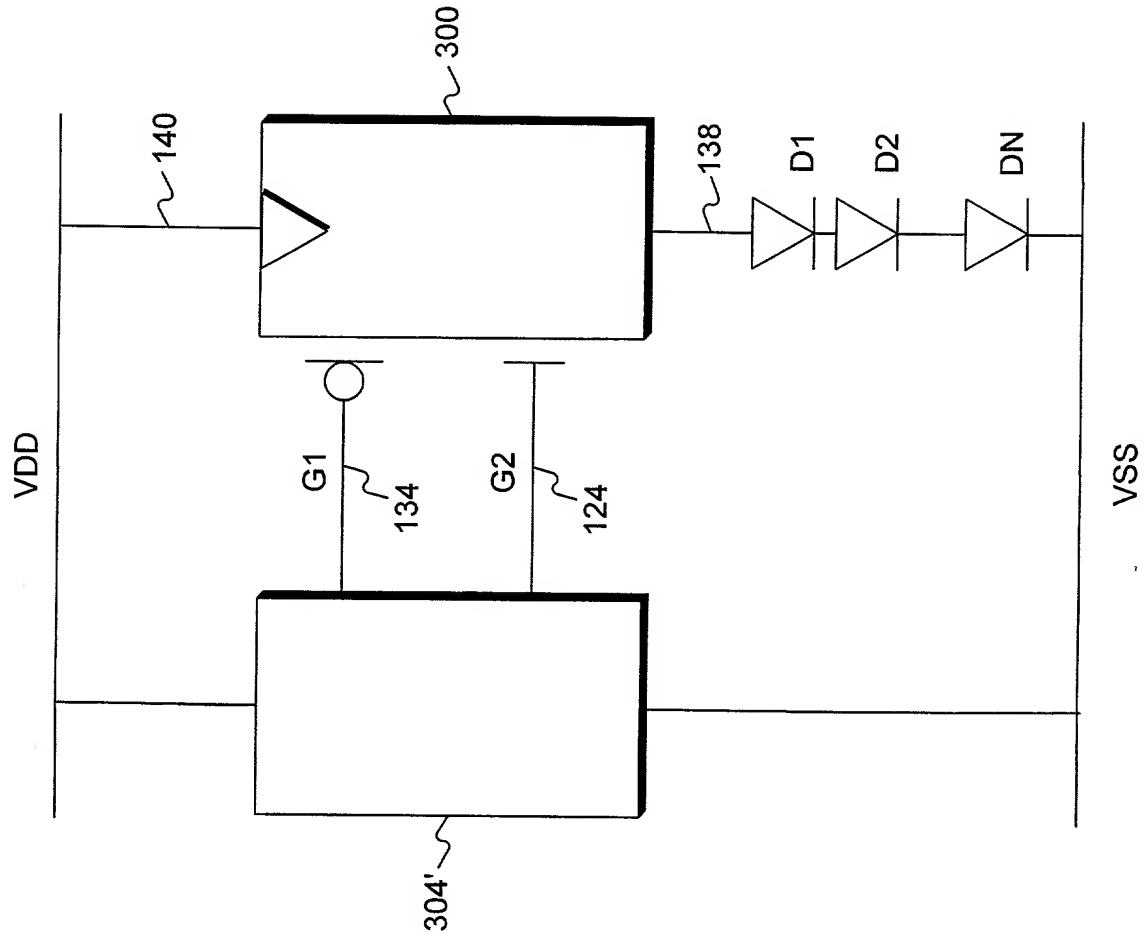


FIG. 8A

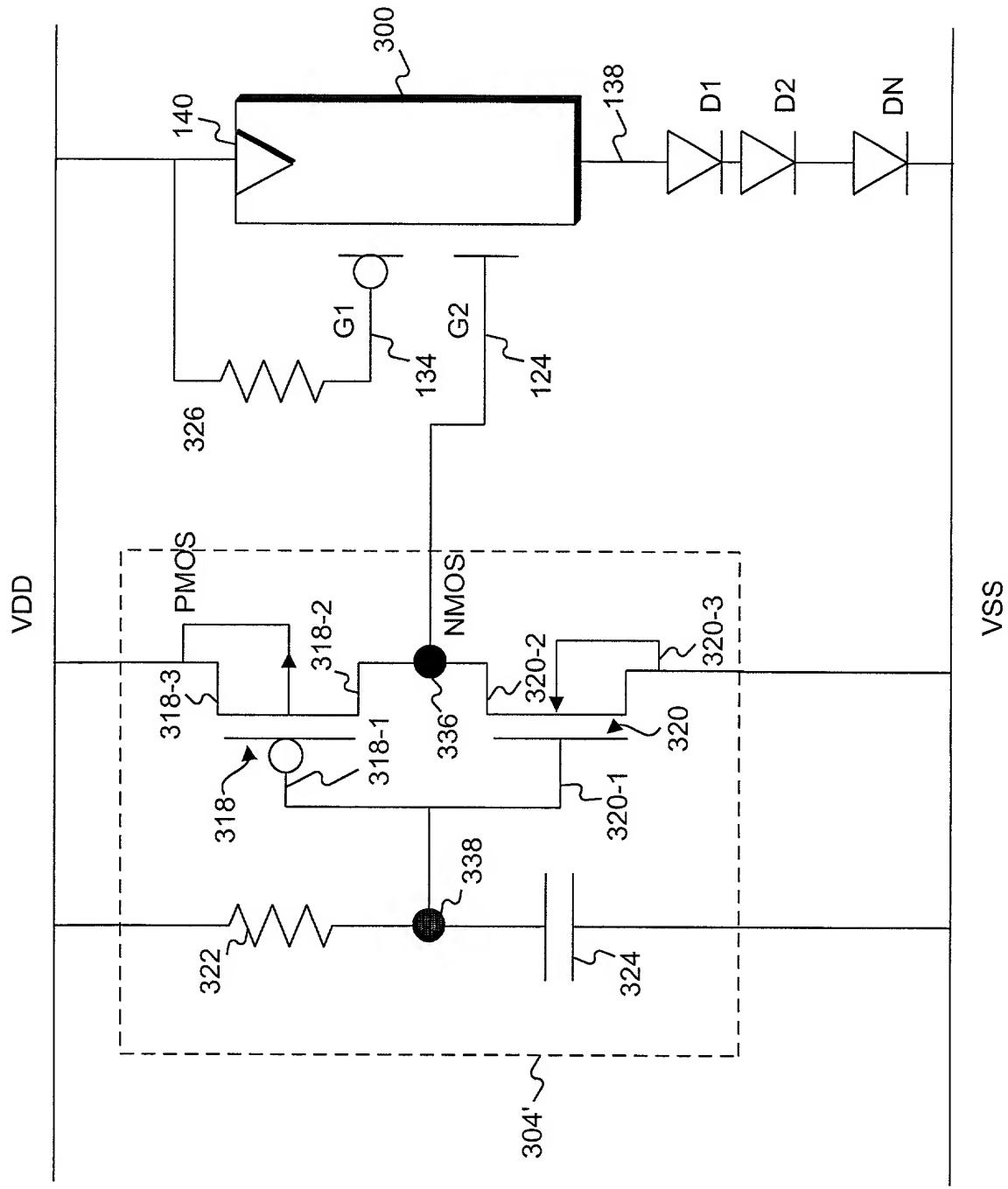


FIG. 8B